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AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method comprising:

if a seize request for an address is an intent seize, finding a first hash table from among a plurality of hash tables, wherein the first hash table is associated with a first processor of a plurality of processors, wherein the first processor initiated the seize request, and wherein each of the plurality of hash tables is associated with a respective one of the plurality of processors;

determining whether the address exists in the first hash table; ~~and~~

if the address exists in the first hash table and the seize request is for the intent seize, obtaining the intent seize via a resource associated with the first processor; and

if the seize request for the address is a non-intent seize, finding a second hash table associated with a second processor of the plurality of processors, wherein the second hash table is designated for all non-intent seizures, regardless of whether the second processor initiated the seize request.

2. (Currently amended) The method of claim 1, further comprising:

if the address does not exist in the first hash table, anchoring the address in the plurality ~~a plurality~~ of hash tables associated with the plurality of processors.

3. (Original) The method of claim 1, further comprising:

if the address does not exist in the first hash table, linking together a plurality of resources associated with the plurality of processors.

4. (Canceled)

5. (Currently amended) The method of claim 1, further comprising: ~~claim 4, further comprising:~~

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anchoring the address in the second hash table if the seize request is for the non-intent seize.

6. (Currently amended) An apparatus comprising:

means for determining whether a seize request for an address is an intent seize;

means for determining a first hash table from among a plurality of hash tables based on a first processor of a plurality of processors, wherein the first processor initiated the seize request if the seize request is for the intent seize, and wherein each of the plurality of hash tables is associated with a respective one of the plurality of processors;

means for determining whether the address exists in a hash class entry in the first hash table; and

means for obtaining the intent seize via a seize control block associated with the first processor if the address exists in the hash class entry and the seize request is for the intent seize; and

means for finding a second hash table associated with a second processor of the plurality of processors, wherein the second hash table is designated for all non-intent seizures, regardless of whether the second processor initiated the seize request.

7. (Currently amended) The apparatus of claim 6, further comprising:

means for anchoring the address in ~~the plurality~~ a plurality of hash tables associated with the plurality of processors if the address does not exist in the hash class entry in the first hash table.

8. (Original) The apparatus of claim 6, further comprising:

means for linking together a plurality of seize control blocks associated with the plurality of processors if the address does not exist in the hash class entry in the first hash table.

9. (Canceled)

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10. (Currently amended) The apparatus of ~~claim 6~~claim 9, further comprising:

means for anchoring the address in the second hash table if the seize request is for the non-intent seize.

11. (Currently amended) A ~~storage signal-bearing~~ medium encoded with instructions, wherein the instructions when executed comprise:

if a seize request for an address is an intent seize, finding a first hash table from among a plurality of hash tables, wherein the first hash table is associated with a first processor of a plurality of processors, wherein the first processor initiated the seize request, and wherein each of the plurality of hash tables is associated with a respective one of the plurality of processors;

determining whether the address exists in the first hash table;

if the address exists in the first hash table and the seize request is for the intent seize, obtaining the intent seize via a seize control block associated with the first processor; and

if the address does not exist in the first hash table and the seize request is for the intent seize, anchoring the address in ~~the plurality~~a plurality of hash tables associated with the plurality of processors; and

if the seize request for the address is a non-intent seize, finding a second hash table associated with a second processor of the plurality of processors, wherein the second hash table is designated for all non-intent seizures, regardless of whether the second processor initiated the seize request.

12. (Currently amended) The ~~storage signal-bearing~~ medium of claim 11, further comprising:

if the address does not exist in the first hash table, linking together a plurality of seize control blocks associated with the plurality of processors.

13. (Canceled)

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14. (Currently amended) The ~~storage signal-bearing~~ medium of claim ~~11-13~~, further comprising:

anchoring the address in the second hash table if the seize request is for the non-intent seize.

15. (Currently amended) The ~~storage signal-bearing~~ medium of ~~claim 11~~ ~~claim 13~~, wherein the intent seize is a less restrictive lock on memory than the non-intent seize.

16. (Currently amended) A computer system comprising:

a plurality of processors; and

a main memory encoded with instructions, wherein the instructions when executed on at least one of the plurality of processors comprise:

if a seize request for an address is an intent seize, finding a first hash table from among a plurality of hash tables, wherein the first hash table is associated with a first processor of the plurality of processors, wherein the first processor initiated the seize request, and wherein each of the plurality of hash tables is associated with a respective one of the plurality of processors,

determining whether the address exists in the first hash table,

if the address exists in the first hash table and the seize request is for the intent seize, obtaining the intent seize via a seize control block associated with the first processor, ~~and~~

if the address does not exist in the first hash table and the seize request is for the intent seize, anchoring the address in ~~the plurality~~ ~~a plurality~~ of hash tables associated with the plurality of processors and linking together a plurality of seize control blocks associated with the plurality of processors, and

if the seize request for the address is a non-intent seize, finding a second hash table associated with a second processor of the plurality of processors,

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wherein the second hash table is designated for all non-intent seizures, regardless of whether the second processor initiated the seize request.

17. (Canceled)

18. (Currently amended) The computer system of claim 16~~claim 17~~, wherein the instructions further comprise:

if the seize request is for the non-intent seize and the address exists in the second hash table, anchoring the address in the second hash table.

19. (Currently amended) The computer system of claim 16~~claim 17~~, wherein the instructions further comprise:

if the seize request is for the non-intent seize and the address does not exist in the second hash table, obtaining the non-intent seize, wherein the obtaining further comprises locking a gate in each of the plurality of the seize control blocks associated with each of the plurality of processors.

20. (Currently amended) The computer system of claim 16~~claim 17~~, wherein the intent seize is a less restrictive lock on memory than the non-intent seize.